REMARKS/ARGUMENTS

In the Final Office Action mailed July 14, 2008, claims 1, 3, 4, and 6 – 9 were rejected. In response, Applicant proposes amending claims 1, 3, and 7. Applicant respectfully requests that the amendments be entered to put the claims in condition for allowance or to put the claims in better condition for appeal. Applicant hereby requests reconsideration of the application in view of the proposed amendments and the below provided remarks.

<u>Response to Claim Rejections</u>

Claims 1, 3, 4, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (U.S. Pat. No. 5,384,570) in view of Applicant's Admitted Prior Art (AAPA), Fig. 2.

Applicant proposes amending claim 1 to recite "a current source (20)" and "a buffering transistor (30)" instead of "level shifting (20) and buffering means (30)." Support for this amendment is found in Applicant's specification at, for example, paragraph [0021], claim 3 as originally filed, and Fig. 5. Additionally, Applicant proposes amending claim 1 to particularly point out "a second bootstrap switch (14b)." Support for this amendment is found in Applicant's specification at, for example, paragraph [0022] and Fig. 5. As amended, claim 1 recites:

> "A single track-and-hold circuit having an input signal (Vin) and an output signal (Vs), a bootstrap switch (14a) having as its inputs a clock signal and an input signal (vin), said input signal (vin) of said bootstrap switch (14a) being connected to said output signal (Vs) of said circuit via a current source (20) and a buffering transistor (30), characterized in that said input signal (vin) of said bootstrap switch (14a) comprises said output signal (Vs) of said circuit; said single track-and-hold circuit further comprising a capacitor (12), said input signal (Vin) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal (clkboot) equal to said input signal (Vin) added to a supply voltage (Vdd); and
>
> including ***a second bootstrap switch (14b), the input signal (vin) of which is connected to said output signal (Vs) of said single track-and-hold circuit <u>via said current source (20) and said buffering transistor (30)</u> of said single track-and-hold circuit.***" (emphasis added)

As recited in amended claim 1, the first and second bootstrap switches are connected to the output signal (Vs) via the current source (20) and the buffering transistor (30). That is, the first and second bootstrap switches are connected to the output signal (Vs) via the same current source (20) and the same buffering transistor (30).

Applicant asserts that claim 1, as amended, is not unpatentable over Dedic in view of the AAPA because neither Dedic nor the AAPA teach or suggest first and second bootstrap switches, wherein both of the bootstrap switches are connected to the output signal (Vs) via the same current source (20) and the same buffering transistor (30).

The Office action cites "4, 5 included in VSC1, VSC2" of Dedic as teaching two or more bootstrap switches. Applicant respectfully points out that VSC1 and VSC2 in Fig. 11 of Dedic represent two separate voltage storage circuits, Dedic col. 25, lines 46 – 48. Although Fig. 11 depicts two bootstrap switched driving devices (4, 5), the two bootstrap switched driving devices (4, 5) are each associated with a different one of the two separate voltage storage devices, VSC1 and VSC2, and with two separate amplifier elements (3). In contrast to Dedic, amended claim 1 recites a single track-and-hold circuit that includes first and second bootstrap switches, where the first and second bootstrap switches are connected to the output signal (Vs) via the same current source and the same buffering transistor. Clearly the two bootstrap switched driving devices (4,5) depicted in Fig. 11 of Dedic are not connected to the output signal via the same amplifier element (3) (where the amplifier element (3) is alleged to include the level shifting and buffering means of claim 1 as previously presented). Because Dedic does not teach first and second bootstrap switches that are connected to an output signal via the same current source and the same buffering transistor, Applicant asserts that amended claim 1 is patentable over Dedic in view of the AAPA.

Dependent Claims 3, 4, and 6 – 9

Claims 3, 4, and 6 – 9 are dependent on claim 1. Applicant respectfully asserts claims 3, 4, and 6 – 9 are allowable at least based on an allowable base claim.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

/mark a. wilson/

Date: September 3, 2008

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111